REMARKS

Claims 1, 4-16 and 21 are rejected under 35 USC 102(a) as being anticipated by Sun et al., US Patent 6,630, 384. Claims 2,3 and 17-20 are rejected under 35 USC 103(a) as being unpatentable over Sun et al. Further, the Examiner cites Gill et al. (US Patent 5,023,680) and Eitan (US Patent 6,201,282).

Sun et al. teaches a method of increasing the core gate density in a non-volatile semiconductor memory device by, generally, depositing an insulation material over a first set of memory cell gates, depositing a polysilicon layer over the insulation material layer and then planarizing the substrate to form a second set of memory cell gates between the first set of memory cell gates.

Gill et al. teaches a control gate horizontally disposed over a floating gate, separated by an insulating layer. A sidewall oxide and a thermally grown oxide are taught to be on the sides of the floating gate and control gates.

Eitan teaches a method of forming dual bit cells through novel masking and doping steps.

The current application provides for a high density multi-bit non-volatile memory device by using conductive sidewall spacers as the control gates.

102(a)

Applicants respectfully submit claims 1, 4-16, and 21 are patentable under 35 U.S. 102(a) over Sun because Sun fails to teach all features of at least independent claim 1, from which claims 4-16 and 21 depend. More specifically, Sun teaches that "an insulation material layer 118 is formed adjacent to the patterned polysilicon gates 116 using any suitable means..." (Col. 6, lines 62-64). Further, Sun teaches that "another insulation layer 120 is formed over the structure 110 using any suitable means...The second insulation material is the same or different from the first insulation material" (Col. 7, lines 25-32).

On page 3 of the Office Action dated January 5, 2005, the Examiner states that Sun anticipates at least claim 1 because Sun discloses a method of "forming a first and second sidewall spacer 120 on two sides of control gate, the first and second spacer control gates is separated from the control gate by insulating liner, and charge storage regions are created within the charge storage layer beneath the control gates". Applicants believe that the insulation layer

120 of Sun cannot be used as a spacer control gate because it is formed from "the second insulation material".

Claims 4-16 and 21 are dependent claims from claim 1. Believing claim 1 to be patentable for the reasons stated above, claims 4-16 and 21 are patentable.

For at least these reasons, claims 1, 4-16 and 21 are patentable over Sun under 35 U.S.C. 102(a).

103(a)

Applicants respectfully submit claims 2,3 and 17-20 are patentable under 35 U.S. 103(a) over Sun because the method of "form(ing) first and second sidewall spacer control gates adjacent to first and second sidewalls of the first control gate..." are not made obvious from Sun. This is the independent claim from which claims 2,3 and 17-20 depend. Believing claim 1 to be allowable for the reasons above, applicants respectfully submit that claims 2, 3 and 17-20 be allowable as well.

The Examiner cites Gill et al. as art of record. The present invention seeks to minimize the dead space in a non-volatile memory array by "form(ing) first and second sidewall spacer control gates adjacent to first and second sidewalls of the first control gate...". In contrast, Gill et al., teaches a method of forming structures having buried bitlines. The gate structure in Gill et al. is stacked and uses dielectric materials for the sidewall spacers. The applicant believe that the claims as originally filed are allowable over Gill et at.

Additionally, the Examiner points to Eitan which is art of record. The applicants respectfully submit that this patent teaches and claims a manufacturing method for a dual bit, mask programmable array and does not teach, nor claim, a method of manufacturing the various gates, specifically by "form(ing) first and second sidewall spacer control gates adjacent to first and second sidewalls of the first control gate...". . The applicants believe that the claims as originally filed are allowable over Eitan.

Conclusion

No amendment made was related to the statutory requirements of patentability unless expressly stated herein. No amendment made was for the purpose of narrowing the scope of any claim, unless the applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Believing to have responded to every issue raised by the Examiner in the last communication mailed, Applicants believe the present application is currently in a condition of allowance.

Applicants earnestly solicit allowance of all pending claims. Please contact Applicant's practitioner listed below if there are any issues.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

SEND CORRESPONDENCE TO:

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